REMARKS

Applicant has reviewed the Office Action mailed on May 8, 2003. Claims 1-133 are pending in this application.

DECLARATION

Applicant submits herewith a supplemental declaration under 37 CFR 1.175(b)(1). Therefore, the rejection based on the defective oath is overcome.

SUPPORT FOR NEW CLAIMS

During the prosecution of this reissue application, Applicant has added new claims 62-133. The following tables refer to sections of the original patent that support these claims. Applicant notes that these tables are not represented as exhaustive. Rather, the tables indicate where Applicants believe there is sufficient support for the new claims. Additional support may be found elsewhere in the original patent.

	Support in Specification
62. A spread spectrum radio transceiver comprising:	Each of the elements of claim 62 is supported by claim 1 of the original patent. Further support is found in Fig. 1 and the description thereof.
a baseband processor and a radio circuit coupled thereto, said baseband processor comprising	Processor 40 and circuitry on left side of Figure 1. Col. 4, line 42-Col. 8, line 46.
a demodulator for spread spectrum phase shift keying (PSK) demodulating information received from said radio circuit,	Demodulator 60 of Figs. 1 and 5. Col. 2, lines 43-46.
at least one analog-to-digital (A/D) converter having an output coupled to said demodulator and an input AC-coupled to said radio circuit,	A/D converter 41 of Fig. 1. Col. 2, lines 43-46. Col. 5, lines 21-23.
said demodulator comprising at least one modified Walsh code function correlator for decoding information according to a modified Walsh code reducing an average DC signal component, and	Walsh Corr 65 of Figs. 5 and 6. Col. 2, lines 46-52. Col. 6, lines 6-34. Col. 7, line 52-Col. 8, line 3.
a modulator for spread spectrum PSK modulating information for transmission via the radio circuit, said modulator comprising at least one modified Walsh code function encoder for encoding information according to the modified Walsh code.	Modified Walsh Generators 53a and 53b of Fig. 2. Col. 2, lines 37-40. Col. 5, line 30 - Col. 7, line 14.

	Support in Specification
63. A spread spectrum radio transceiver according to claim 62 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and	Claim 2. Col. 2 lines 56-59. Col. 5, lines 37-53.
wherein said demodulator is configured to operate in one of the first and second formats.	Claim 2. Col 2, lines 60-61.

	Support in Specification
64. A spread spectrum radio transceiver according to claim 63 wherein said modulator is configured to modulate data packets to include a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and	Claim 3. Col. 2, lines 61-66. Col. 6, line 48 - Col. 7, line 14.
wherein said demodulator is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.	Claim 3. Col. 2, line 66 - Col. 3, line 3. Col. 6, line 48 - Col. 7, line 14.

	Support in Specification
65. A spread spectrum radio transceiver according to claim 64 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.	Claim 4. Col. 3, lines 3-5.

	Support in Specification
66. A spread spectrum radio transceiver according to claim 64 wherein said demodulator further comprises:	Claim 5 supports all of the limitations of claim 66.
a first carrier tracking loop for the third format; and	Col. 3, lines 6-9. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a second carrier tracking loop for the first and second formats.	Col. 3, lines 6-9. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
67. A spread spectrum radio transceiver according to claim 66 wherein said second carrier tracking loop comprises:	Claim 6 supports all of the limitations of claim 67.
a carrier numerically controlled oscillator (NCO); and	Col. 3, lines 9-14. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.	Col. 3, lines 9-14. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
68. A spread spectrum radio transceiver according to claim 66 wherein said second carrier tracking loop comprises:	Claim 7 supports all of the limitations of claim 68.
a carrier loop filter; and	Col. 3, lines 14-20. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.	Col. 3, lines 14-20. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
69. A spread spectrum radio transceiver according to claim 62 wherein said modulator is further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one modified Walsh code function encoder.	Claim 8. Col. 3, lines 27-30. Col. 5, line 60 - Col. 6, line 5.

	Support in Specification
70. A spread spectrum radio transceiver according to claim 62 wherein the modified Walsh code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.	Claim 9. Col. 3, lines 25-27. Col. 6, lines 28-34.

	Support in Specification
71. A spread spectrum radio transceiver according to claim 62 wherein said at least one modified Walsh code function correlator comprises:	Claim 10 supports all of the limitations of claim 71.
a modified Walsh function generator; and	Generator 81 of Fig. 6. Col. 7, lines 55-57.
a plurality of parallel coupled correlators coupled to said modified Walsh function generator.	Correlators 65 of Fig. 6. Col. 7, lines 55-57.

	Support in Specification
72. A spread spectrum radio transceiver according to claim 62 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is configured to generate a preamble; and	Claim 11. Col. 3, lines 31-35.
wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.	Claim 11. Col. 3, lines 31-35.

	Support in Specification
73. A spread spectrum radio transceiver according to claim 62 wherein said modulator comprises a scrambler; and	Claim 12. Col. 3, lines 38-39. Col. 5, lines 60-63.
wherein said demodulator comprises a descrambler.	Claim 12. Col. 3, lines 39-40. Col. 7, lines 30-34.

	Support in Specification
74. A spread spectrum radio transceiver according to claim 62 wherein said demodulator is configured to generate a clear channel assessment signal.	Claim 13. Col. 3, lines 40-43.

	Support in Specification
75. A spread spectrum radio transceiver according to claim 62 wherein said radio circuit comprises:	Claim 14 supports all of the limitations of claim 75.
a quadrature intermediate frequency modulator/demodulator coupled to said baseband processor; and	QUAD IF MOD/DEMOD 35 of Fig. 1. Col. 3, lines 47-49. Col. 4, lines 61-63.
an up/down frequency converter coupled to said quadrature intermediate frequency modulator/demodulator.	UP/DOWN CONVERTER 33 of Fig. 1. Col. 3, lines 49-51. Col. 4, lines 61-63.

	Support in Specification
76. A spread spectrum radio transceiver according to claim 75 wherein said radio circuit further comprises:	Claim 15 supports all of the limitations of claim 76.
a low noise amplifier having an output coupled to an input of said up/down converter; and	LNA 38 of Fig.1 . Col. 3, lines 51-53. Col. 4, lines 56-59.
a radio frequency power amplifier having an input coupled to an output of said up/down converter.	LNA 38 of Fig.1 . Col. 3, lines 53-55. Col. 4, lines 56-59.

	Support in Specification
77. A spread spectrum radio transceiver according to claim 76 further comprising:	Claim 16 supports the limitations of claim 77.
an antenna; and	Antenna 31 of Fig. 1. Col. 3, lines 55-59. Col. 4, lines 48-53.
an antenna switch for switching said antenna between the output of said radio frequency power amplifier and the input of said low noise amplifier.	Switch of Fig. 1. Col. 3, lines 55-59. Col. 4, lines 48-53.

	Support in Specification
78. A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:	Each of the elements of claim 78 is supported by claim 17 of the original patent. Further support is found in Fig. 1 and the description thereof.
a demodulator for spread spectrum phase shift keying (PSK) demodulating;	Demodulator 60 of Figs. 1 and 5. Col. 2, lines 43-46.
at least one analog-to-digital (A/D) converter having an output coupled to said demodulator and an input AC-coupled to receive information;	A/D converter 41 of Fig. 1. Col. 2, lines 43-46. Col. 5, lines 21-23.
said demodulator comprising at least one orthogonal code function correlator for decoding information according to an orthogonal code reducing an average DC signal component to thereby increase AC-coupling to said at least one A/D converter; and	Walsh Corr 65 of Figs. 5 and 6. Col. 2, lines 46-52. Col. 5, lines 37-53. Col. 6, lines 6-34. Col. 7, line 52-Col. 8, line 3.
a modulator for spread spectrum PSK modulating information for transmission, said modulator comprising at least one orthogonal code function encoder for encoding information according to the orthogonal code.	Modified Walsh Generators 53a and 53b of Fig. 2. Col. 2, lines 37-40. Col. 5, line 30 - Col. 7, line 14.

	Support in Specification
79. A baseband processor according to claim 78 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and	Claim 18. Col. 2 lines 56-59. Col. 5, lines 37-53.
wherein said demodulator is configured to operate in one of the first and second formats.	Claim 18. Col 2, lines 60-61.

	Support in Specification
80. A baseband processor according to claim 79 wherein said modulator is configured to modulate data packets to include a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and	Claim 19. Col. 2, lines 61-66. Col. 6, line 48 - Col. 7, line 14.
wherein said demodulator comprises is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.	Claim 19. Col. 2, line 66 - Col. 3, line 3. Col. 6, line 48 - Col. 7, line 14.

	Support in Specification
81. A baseband processor according to claim 80 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.	Claim 20. Col. 3, lines 3-5.

	Support in Specification
82. A baseband processor according to claim 80 wherein said demodulator further comprises:	Claim 21 supports all of the limitations of claim 66.
a first carrier tracking loop for the third format; and	Col. 3, lines 6-9. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a second carrier tracking loop for the first and second formats.	Col. 3, lines 6-9. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
83. A baseband processor according to claim 82 wherein said second carrier tracking loop comprises:	Claim 22 supports all of the limitations of claim 67.
a carrier numerically controlled oscillator (NCO); and	Col. 3, lines 9-14, Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.	Col. 3, lines 9-14, Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
84. A baseband processor according to claim 82 wherein said second carrier tracking loop comprises:	Claim 23 supports all of the limitations of claim 68.
a carrier loop filter; and	Col. 3, lines 14-20. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a controller to selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.	Col. 3, lines 14-20. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
85. A baseband processor according to claim 78 wherein said modulator is further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one orthogonal code function encoder.	Claim 24. Col. 3, lines 27-30. Col. 5, line 60 - Col. 6, line 5.

	Support in Specification
86. A baseband processor according to claim 78 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.	Claim 25. Col. 3, lines 25-27. Col. 6, lines 28-34.

	Support in Specification
87. A baseband processor according to claim 78 wherein the orthogonal code is a bi-orthogonal code.	Claim 26. Col. 5, lines 37-53.

	Support in Specification
88. A baseband processor according to claim 78 wherein said at least one orthogonal code function correlator comprises:	Claim 27 supports all of the limitations of claim 88.
a predetermined orthogonal code function generator; and	Generator 81 of Fig. 6. Col. 7, lines 55-57.
a plurality of parallel coupled correlators coupled to said orthogonal code function generator.	Correlators 65 of Fig. 6. Col. 7, lines 55-57.

	Support in Specification
89. A baseband processor according to claim 78 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is configured to generate a preamble; and	Claim 28. Col. 3, lines 31-35.
wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.	Claim 28. Col. 3, lines 31-35.

	Support in Specification
90. A baseband processor according to claim 78 wherein said modulator comprises a scrambler; and	Claim 29. Col. 3, lines 38-39. Col. 5, lines 60-63.
wherein said demodulator comprises a descrambler.	Claim 29. Col. 3, lines 39-40. Col. 7, lines 30-34.

	Support in the Specification
91. A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:	Claim 30 supports all of the limitations of claim 91.
a modulator for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator comprising	Modified Walsh Generators 53a and 53b of Fig. 2. Col. 2, lines 37-40. Col. 5, line 30 - Col. 7, line 14.
at least one encoder for encoding information for transmission,	Modified Walsh Generators 53a and 53b of Fig. 2. Col. 2, lines 37-40. Col. 5, line 30 - Col. 7, line 14.
wherein said modulator is configured to operate in one of a first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate, and	Col. 2 lines 56-59. Col. 5, lines 37-53.
wherein said modulator is configured to modulate data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and	Col. 2, lines 61-66. Col. 6, line 48 - Col. 7, line 14.
a demodulator for spread spectrum PSK demodulating received information, said demodulator comprising	Demodulator 60 of Figs. 1 and 5. Col. 2, lines 43-46.
at least one correlator for decoding received information,	Walsh Corr 65 of Figs. 5 and 6. Col. 2, lines 46-52. Col. 6, lines 6-34. Col. 7, line 52-Col. 8, line 3.
wherein said demodulator is configured to operate in one of the first and second formats,	Col 2, lines 60-61.
wherein said demodulator is configured to demodulate data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header,	Col. 2, line 66 - Col. 3, line 3. Col. 6, line 48 - Col. 7, line 14.
a first carrier tracking loop for the third format, and	Col. 3, lines 6-9. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a second carrier tracking loop for the first and second formats.	Col. 3, lines 6-9. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
92. A baseband processor according to claim 91 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.	Claim 31. Col. 3, lines 3-5.

	Support in Specification
93. A baseband processor according to claim 91 wherein said second carrier tracking loop comprises:	Claim 32 supports all of the limitations of claim 93.
a carrier numerically controlled oscillator (NCO); and	Col. 3, lines 9-14. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a controller for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.	Col. 3, lines 9-14. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
94. A baseband processor according to claim 91 wherein said second carrier tracking loop comprises:	Claim 33 supports all of the limitations of claim 94.
a carrier loop filter; and	Col. 3, lines 14-20. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.	Col. 3, lines 14-20. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
95. A baseband processor according to claim 91 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is further configured to generate a preamble; and	Claim 34. Col. 3, lines 31-35.
wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.	Claim 34. Col. 3, lines 31-35.

	Support in Specification
96. A baseband processor according to claim 91 wherein said modulator comprises a scrambler; and	Claim 35. Col. 3, lines 38-39. Col. 5, lines 60-63.
wherein said demodulator comprises a descrambler.	Claim 35. Col. 3, lines 39-40. Col. 7, lines 30-34.

	Support in Specification
97. A modulator for a spread spectrum radio transceiver, said modulator configured to modulate information for transmission by spread spectrum phase shift keying (PSK), said modulator comprising at least one orthogonal code function encoder for encoding information according to an orthogonal code for reducing an average DC signal component.	Claim 36. Modified Walsh Generators 53a and 53b of Fig. 2. Col. 2, lines 37-40. Col. 5, line 30 - Col. 7, line 14. (Col. 5, lines 37-57).

	Support in Specification
98. A modulator according to claim 97 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.	Claim 37. Col. 2 lines 56-59. Col. 5, lines 37-53.

	Support in Specification
99. A modulator according to claim 98 wherein said modulator is configured to modulate data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats.	Claim 38. Col. 2, lines 61-66. Col. 6, line 48 - Col. 7, line 14.

	Support in Specification
100. A modulator according to claim 99 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.	Claim 39. Col. 3, lines 3-5.

	Support in Specification
101. A modulator according to claim 97 wherein said modulator is configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one orthogonal code function encoder, and	Claim 40. Col. 3, lines 27-30. Col. 5, line 60 - Col. 6, line 5.
wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.	Claim 40. Col. 3, lines 25-27. Col. 6, lines 28-34.

	Support in Specification
102. A modulator according to claim 97 wherein said at least one orthogonal code function correlator comprises:	Claim 41 supports all of the limitations of claim 102.
an orthogonal code function generator; and	Generator 81 of Fig. 6. Col. 7, lines 55-57.
a plurality of parallel coupled correlators coupled to said orthogonal code function generator.	Correlators 65 of Fig. 6. Col. 7, lines 55-57.

	Support in Specification
103. A modulator according to claim 97 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.	Claim 42. Col. 3, lines 25-27. Col. 6, lines 28-34.

	Support in Specification
104. A modulator according to claim 97 wherein the orthogonal code is a bi-orthogonal code.	Claim 43. Col. 5, lines 37-53.

	Support in Specification
105. A demodulator for a spread spectrum radio transceiver, said demodulator configured to demodulate information for by spread spectrum phase shift keying (PSK) said demodulator for spread spectrum phase shift keying (PSK) demodulating information received from a radio circuit, said demodulator means comprising at least one orthogonal code function correlator for decoding information according to an orthogonal code reducing an average DC signal component.	Claim 44. Modified Walsh Generators 53a and 53b of Fig. 2. Col. 2, lines 37-40. Col. 5, line 30 - Col. 7, line 14. (Col. 5, lines 37-53).

	Support in Specification
106. A demodulator according to claim 105 wherein said demodulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.	Claim 45. Col. 2 lines 56-59. Col. 5, lines 37-53.

	Support in Specification
107. A demodulator according to claim 106 wherein said demodulator is configured to demodulate data packets including a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats, and for switching to the respective one of the first and second formats of the variable data after the header.	Claim 46. Col. 2, lines 61-66. Col. 6, line 48 - Col. 7, line 14. Col. 2, line 66 - Col. 3, line 3. Col. 6, line 48 - Col. 7, line 14.

	Support in Specification
108. A demodulator according to claim 107 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.	Claim 47. Col. 3, lines 3-5.

	Support in Specification
109. A demodulator according to claim 107 wherein said demodulator further comprises:	Claim 48 supports all of the limitations of claim 109.
a first carrier tracking loop for the third format; and	Col. 3, lines 6-9. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a second carrier tracking loop for the first and second formats.	Col. 3, lines 6-9. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
110. A demodulator according to claim 109 wherein said second carrier tracking loop comprises:	Claim 49 supports all of the limitations of claim 110.
a carrier numerically controlled oscillator (NCO); and	Col. 3, lines 9-14. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.	Col. 3, lines 9-14. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
111. A demodulator according to claim 109 wherein said second carrier tracking loop comprises:	Claim 50 supports all of the limitations of claim 111.
a carrier loop filter; and	Col. 3, lines 14-20. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.
a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.	Col. 3, lines 14-20. Figs. 5 and 7. Col. 7, lines 21-51. Col. 8, lines 4-16.

	Support in Specification
112. A demodulator according to claim 105 further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits).	Claim 51. Col. 3, lines 27-30. Col. 5, line 60 - Col. 6, line 5.

	Support in Specification
113. A demodulator according to claim 105 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.	Claim 52. Col. 3, lines 25-27. Col. 6, lines 28-34.

	Support in Specification
114. A demodulator according to claim 105 wherein the orthogonal code is a bi-orthogonal code.	Claim 53. Col. 5, lines 37-53.

	Support in Specification
115. A demodulator according to claim 105 wherein said at least one orthogonal code function correlator comprises:	Claim 54 supports all of the limitations of claim 115.
an orthogonal code function generator; and	Generator 81 of Fig. 6. Col. 7, lines 55-57.
a plurality of parallel coupled correlators coupled to said orthogonal code function generator.	Correlators 65 of Fig. 6. Col. 7, lines 55-57.

	Support in Specification
116. A method for baseband processor for spread spectrum radio communication, the method comprising:	Claim 55 supports all of the limitations of claim 116.
spread spectrum phase shift keying (PSK) modulating information for transmission while encoding the information according to the orthogonal code for reducing an average DC signal component; and	Modified Walsh Generators 53a and 53b of Fig. 2. Col. 2, lines 37-40. Col. 5, line 30 - Col. 7, line 14.
spread spectrum PSK demodulating received information by decoding the received information according to the orthogonal code.	Walsh Corr 65 of Figs. 5 and 6. Col. 2, lines 46-52. Col. 5, lines 37-53. Col. 6, lines 6-34. Col. 7, line 52-Col. 8, line 3.

	Support in Specification
117. A method according to claim 116 further comprising AC-coupling received information for spread spectrum PSK demodulating so that the reduced average DC signal component in combination with the AC-coupling enhances overall performance.	Claim 56. A/D converter 41 of Fig. 1. Col. 2, lines 43-46. Col. 5, lines 21-23.

	Support in Specification
118. A method according to claim 116 further comprising modulating and demodulating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.	Claim 57. Col. 2 lines 56-59. Col. 5, lines 37-53.

	Support in Specification
119. A method according to claim 118 further comprising: modulating data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and	Claim 58. Col. 2, lines 61-66. Col. 6, line 48 - Col. 7, line 14.
demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.	Claim 58. Col. 2, line 66 - Col. 3, line 3. Col. 6, line 48 - Col. 7, line 14.

	Support in Specification
120. A method according to claim 119 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.	Claim 59. Col. 3, lines 3-5.

	Support in Specification
121. A method according to claim 116 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.	Claim 60. Col. 3, lines 25-27. Col. 6, lines 28-34.

	Support in Specification
122. A method according to claim 116 wherein the orthogonal code is a bi-orthogonal code.	Claim 61. Col. 5, lines 37-53.

	Support in Specification
123. A method of generating an rf signal for transmitting binary information in a packet format including a header field followed by a data field, comprising the steps of:	Fig. 3. Col. 6, line 48 - Col. 7, line 14.
spread spectrum encoding a sequence of first data symbols from said binary information within said header field by combining said first data symbols with a spreading sequence generated at a predetermined chip rate;	Col. 6, line 64-66.
encoding a sequence of N-bit second data symbols, where N is greater than 1, from said binary information within said data field by generating for each of said N-bit second data symbols one of a set of 2^N chip sequences generated at the same chip rate as said spreading sequence; and	Col. 5, line 37 - Col. 6, line 33. Fig. 2.
applying the spread-spectrum encoded symbols of said header field and the selected chip sequences of said data field to the I and Q inputs of a phase shift modulator to produce said rf signal.	Col. 6, lines 34 - 47. Col. 7, lines 5-14. Modulator 50 and Quad IF Mod/Demod 35 of Figure 1.

	Support in Specification
124. The method of claim 123 wherein each said chip sequence is generated by selecting an initial chip sequence in accordance with a first data segment of an N-bit second data symbol and differentially phase encoding said initial chip sequence in accordance with a second data segment of the same N-bit second data symbol.	Col. 6, lines 6-25.

	Support in Specification
125. A method of generating an rf signal for transmitting binary information in a packet format including a header field followed by a data field, comprising the steps of:	Fig. 3. Col. 6, line 48 - Col. 7, line 14.
spread spectrum encoding a sequence of first data symbols from said binary information within said header field by combining said first data symbols with a spreading sequence;	Col. 6, line 64-66.
encoding a sequence of N-bit second data symbols, where N is greater than 1, from said binary information within said data field by generating for each of said N-bit second data symbols one of a set of 2^N chip sequences, each of said chip sequences being differentially phase encoded;	Col. 5, line 37 - Col. 6, line 33. Fig. 2.
applying a reference phase based on encoding of the last of said first data symbols to the differential encoding of the first selected chip sequence; and	Diff Encode Init State from 51. Col. 6, lines 34-35. Col. 7, lines 6-8.
inputting said encoded symbols of said header field and said differentially encoded chip sequences of said data field to the I and Q inputs of a phase shift modulator to produce said rf signal.	Col. 6, lines 34-47. Col. 7, lines 5-14.

	Support in Specification
126. The method of claim 125 wherein each said chip sequence is generated by selecting an initial chip sequence in accordance with a first data segment of an N-bit second data symbol and differentially phase encoding said initial chip sequence in accordance with a second data segment of the same N-bit second data symbol.	Col. 6, lines 6-25.

	Support in Specification
127. A method of generating an rf signal in a transmitter having a phase shift modulator with I and Q inputs comprising the steps of:	
supplying a stream of binary information containing header data and payload data, said header data specifying at least a first payload data rate or a second payload data rate;	Fig. 3. Col. 6, line 48 - Col. 7, line 14.
encoding said payload data when said header data specifies said first payload data rate by grouping said payload data into N-bit symbols, where N is greater than 1, and applying each N-bit symbol to select one of 2^N possible chip sequences;	Col. 5, lines 37-45, 61-63. Col. 6, lines 2-25.
encoding said payload data when said header data specifies said second payload data rate by grouping said payload data into 2N-bit symbols and applying each 2N-bit symbol to select one of 2^{2N} possible chip sequences; and	Col. 5, lines 43-53, Col. 5, line 60 - Col. 6, line 2, Col. 6, lines 6-33.
applying each selected chip sequence to the I and Q inputs of said phase shift modulator.	Col. 6, lines 34 - 47. Col. 7, lines 5-14. Modulator 50 and Quad IF Mod/Demod 35 of Figure 1.

	Support in Specification
128. The method of claim 127 wherein the chip sequences selectable by said 2N-bit symbols include the chip sequences selectable by said N-bit symbols plus 2^{2N}-2^N additional chip sequences.	Col. 5, lines 43-53, Col. 5, line 60 - Col. 6, line 2, Col. 6, lines 6-33.

	Support in Specification
129. The method of claim 127 wherein the chip sequences selected by said N-bit symbols and said 2N-bit symbols are generated by selecting an initial chip sequence in accordance with a first data segment of an N-bit or 2N-bit symbol and differentially phase encoding the selected initial chip sequence in accordance with a second data segment of the same N-bit or 2N-bit symbol.	Col. 6, lines 6-26.

	Support in Specification
130. The method of claim 127 wherein each of the 2^{2N} chip sequences selectable by said 2N-bit symbols comprises an I/Q chip sequence having an I segment and a Q segment adapted to be synchronously applied to said I and Q inputs, respectively.	Col. 6, lines 40-47.

	Support in Specification
131. The method of claim 129 wherein N=4 and wherein each chip sequence selected by a 2N-bit symbol comprises an initial I/Q chip sequence having an I segment and a Q segment adapted to be synchronously applied to said I and Q inputs, respectively, said initial I/Q chip sequence being selected by 6 bits of a 2N-bit symbol and being differentially phase encoded in accordance with the other 2 bits of the same 2N-bit symbol.	Col. 5, lines 43-53, Col. 5, line 60 - Col. 6, line 2, Col. 6, lines 6-33.

	Support in Specification
132. A method of encoding binary data for transmission in packet format along with information encoded at a predetermined spread spectrum chip rate, said method comprising the steps of:	Fig. 3. Col. 6, line 48 - Col. 7, line 14.
grouping said binary data into N-bit symbols;	Col. 5, lines 37 - 39, 46-48.
applying a K-bit segment of each N-bit symbol to a chip sequence generator to select one of 2^K chip sequences, wherein each chip sequence is M chips in length and is a composite of an M-bit basic sequence and an M-bit modification sequence;	Col. 6, lines 6-20.
rotating the phase of the selected chip sequence in accordance with an N-K bit segment of the same N-bit symbol that selected said chip sequence; and	Col. 6, lines 21-25.
transmitting each phase-rotated, selected chip sequence at said predetermined chip rate.	Col. 6, lines 40-47.

	Support in Specification
133. A method of encoding binary data for transmission in packet format along with information encoded at a predetermined spread spectrum chip rate, said method comprising the steps of:	Fig. 3. Col. 6, line 48 - Col. 7, line 14.
grouping said binary data into N-bit symbols;	Col. 5, lines 37 - 39, 46-48.
applying a K-bit segment of each N-bit symbol to a chip sequence generator to select one of 2^K chip sequences, wherein each chip sequence is M chips in length;	Col. 6, lines 6-20.
combining the selected basic chip sequence with a fixed, M-chip modification sequence to produce a selected M-chip composite chip sequence;	Col. 6, lines 6-20.
rotating the phase of the selected M-chip composite chip sequence in accordance with an N-K bit segment of the same N-bit symbol that selected said basic chip sequence; and	Col. 6, lines 21-25.
transmitting each phase rotated, selected composite chip sequence at said predetermined chip rate.	Col. 6, lines 40-47.

CONCLUSION

Applicant respectfully submits that claims 1-133 are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 332-4720.

Respectfully submitted,

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